In the Specification:

Please replace the paragraph beginning on page 03, line 08, and ending on page 03, line 20, with the following:

Referring to FIG. 1A, a master/slave latch 10 is employed to prevent data from logic stage 11 from propagating through latch 10 before a logic stage 12 is ready to act on the data. Master/slave latch 10 includes a master latch 18 and a slave latch 20. Master latch 18 empties data into slave latch ~~18~~ 20 in accordance with global clock signals. Switches 14 and 16 of latch 10 are enabled by global clock pulses C1 and C2, respectively, to transfer data (Data) across latch 10 as shown in FIG. 1B which shows a timing diagram. Unfortunately, the master slave approach has to deal with clock skew and jitter and consumes more power in the clocking to drive both the master and the slave latches.

Please replace the paragraphs beginning on page 14, line 7, and ending on page 15, line 08, with the following:

Referring to FIG. 6, a multiple stage pipeline 300 is shown in accordance with one embodiment of the present invention. Pipeline 300 is an asynchronous pipeline. Stages 301, 302 and 303 each include a latch stage 304 for temporary storage of data which passes from stage to stage through pipeline 300. Latch stages 304a, 304b and 304c are interposed between logic circuits ~~306~~ 306a, 306b, 306c for each stage. Latch stages 304a, 304b and 304c are each enabled by a separate locally generated clock signal (CLKEi, CLKEj and CLKEk, respectively).

When CLKEi is enabled, latch 304a simultaneously captures that data that is at its input and launches this data into logic ~~306~~306a. In addition, CLKEi launches the

valid signal VALIDi which goes to interlock block 330b. Interlock block 330b is activated causing CLKEj to be enabled when both VALIDi and ACKk have occurred. When CLKEj is enabled, latch 304b simultaneously captures the data at its input from the output of logic ~~306~~ 306a in stage 301 and launches that data into logic ~~306~~ 306b of stage 302. In addition, CLKEj launches the valid signal VALIDj which goes to interlock block 330b in stage 303. The process is continued for each stage in the pipeline 300. Local clock circuits 330a, 330b and 330c are employed for generating and receiving handshaking interlock signals, VALID and ACK.

Please replace the paragraphs beginning on page 17, line 03, and ending on page 18, line 02, with the following:

Referring to FIGS. 9A and 9B, a strobe or local clock circuit 500 is shown in accordance with an illustrative embodiment of the present invention. Invertors 501, n-[[ ]]channel devices 503a and 503b, latches 504, and p-channel devices 505a and 505b may be connected, replaced or otherwise altered as known by one skilled in the art. The operation of strobe circuit 500 can be understood by starting at the end of a cycle when external valid signals (VALID1 to VALIDi) and CLKR which is generated from the acknowledge signals (ACK) are low, switches 502 are open, and the internal valid signals (Vint1 to Vinti) and Rint are high. The strobe outputs, CLKE and ACK, which are high and low respectively, will transition to low and high respectively only when all of the internal valid signals (Vint1 to Vinti) and Rint go low. For this to happen, each external valid signal (VALID1 to VALIDi) is first reset high, thereby turning on its associated switch 502. Next, each of the valid inputs (VALID1 to VALIDi) will transition low, as data for that input becomes valid. This causes the associated internal valid

signal (Vint1 to Vinti) to also go low. CLKEN is the falling clock signal having opposite polarity of CLKE.

Please replace the paragraphs beginning on page 18, line 11, and ending on page 19, line 02, with the following:

ACK is also the handshaking signal to stages or blocks transmitting data. The ACK signal represents that data has been received and the blocks can send more data. Immediately after ACK turns switch 502 off, CLKEN will precharge each of the internal valid nodes (Vint) and Rint high. This in turn will cause ACK and CLKE to go low and CLKEN to go high. In the strobe circuit 500 of FIG. 9A, a p-channel load device 505a of a static NOR 506, also comprising n-channel devices 503a, is connected to only one internal Valid signal (Vinti). The Valid signal to which the load is connected should be the nominally last arriving. However, in actual operation if another signal arrives last the circuit will function normally but with some additional power dissipation. A node X is labeled in FIGS. 9A and 9B to provide a reference between the FIGS.